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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/443,160	11/19/1999	DAVID L. ISAMAN	98-MET-069	6854

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STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
ALROBAYE, IDRISS N	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/443,160	ISAMAN, DAVID L.	
	Examiner	Art Unit	
	IDRISS N. ALROBAYE	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,6-13 and 16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-3, 6-13, 16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communications through the applicant's application filed on 12/16/2008.

2. Claims 2-3, 6-13, 16-21 remained for examination. Claims 1, 4-5 and 14-15 are canceled.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/16/2008 has been entered.

Claims and Remarks

4. Each page of the response (claims and remarks) shows the serial number as 10/611,153. It should be corrected to **09/443,160**.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first and second paragraphs of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
>
> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 2-3, 6-13 and 16-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

7. As per claims 2-3, 12-13, the "detection based upon the base and offset address values" and "without using memory address corresponding to the base and offset address values" appears to be a new matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventors, at the time the application was filed, has possession of the claimed invention.

8. Claims 2-3, 6-13 and 16-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. As per claims 2 and 12, taking claim 2 as exemplary, the claim recites "***detecting*** *a first instruction* ***using first base and offset address values*** *to load data from a first memory location that was previously stored to,* ***wherein*** *the first instruction is* ***detected based upon the first base and offset address*** *values and* ***without*** *using a memory address corresponding to* ***the first base and offset address values.***" The claim

appears to be vague and indefinite. The claim appears to contradict itself, it detects the first instruction using the base and offset address value and later in the claim the detection is based on the base and offset but without using the address corresponding to the first base and offset address values. Thus, it is not clear how it is detecting based on the base and offset address values but not using them. Appropriate correction/clarification is required.

10. As per claims 3 and 13, they are rejected for the same reasoning as set forth above in claim 2.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 2, 12 and 20 are rejected under 35 U.S.C. 102 (b) as being anticipated by Yeager U.S. Patent No. 6,216,200.

13. As per claim 20, Yeager teaches a method for operating a pipelined microprocessor, comprising:

detecting a first instruction that stores data to a first memory location (see col. 8, lines 1-14, "store instruction"), the first instruction comprising syntax for computing an

effective address for the first memory location (see col. 5, lines 13-26, wherein "virtual address" is equivalent to syntax; see also col. 9, lines 18-39, "offset" is equivalent to effective address);

detecting a second instruction that loads data from a second memory location (see col. 28, lines 54-65, "load instruction"), the second instruction comprising syntax for computing an effective address for said second memory location (see col. 5, lines 13-26, wherein "virtual address" is equivalent to syntax; see also col. 9, lines 18-39, "offset" is equivalent to effective address);

determining the syntax for said the first instruction and the syntax for said the second instruction (see col. 30, lines 43-49 comparison of "virtual addresses");

using the syntax for said the first instruction and said the syntax for the second instruction to determine a relationship between the first memory location and the second memory location (see col. 30, lines 43-49 comparison of "virtual addresses" to see if there's store-to-load dependency), without using the effective address for the first memory location or the effective address for the second memory location (see col. 30, lines 43-49. First virtual address are not effective addresses, thus it's "without using the effective addresses". Second, this limitation is interpreted as without using effective address to access memory which is shown in col. 30, lines 43-65); and

using the relationship to determine whether to perform one of the first instruction and the second instruction (col. 30, lines 43-65).

14. As per claim 2, Yeager teaches a pipelined microprocessor detecting a first instruction using first base and offset address values to load data from a first memory location that was previously stored to (see col. 28, lines 54-65 "load and store"; see col. 5, lines 13-26 and col. 9, lines 18-39, "offset" and "base"), wherein the first instruction is detected based upon the first base and offset address values (see col. 30, lines 43-49 "comparison of virtual addresses") and without using a memory address corresponding to the first base and offset address values (see col. 30, lines 43-49 comparison of "virtual addresses" to see if there's store-to-load dependency; see also col. 30, lines 43-49. First, virtual addresses are not memory addresses corresponding to base and offset address values, thus reads on the limitation. Second, this limitation is interpreted as without using base and offset to access memory location which is shown in col. 30, lines 43-65).

15. As per claim 12, it is rejected for the same reasons set forth above in claim 2.

16. Claims 2-3, 6-13, 16-21 are rejected under 35 U.S.C. 102 (b) as being anticipated by Hesson et al. U.S. Patent No. 5,666,506 (hereinafter Hesson).

17. As to claim 2, 12, Hesson taught at least:

A pipelined microprocessor (see pipeline processor in col. 1, lines 29-34 for background) detecting a first instruction using first base and offset address values to load data from a first memory location that was previously stored to (see comparison of

instruction in col. 4, lines 64-67 and col. 5, lines 1-13, wherein the virtual address has a base and effective address), wherein the first instruction is detected based upon the first base and offset address value and without using a memory address corresponding to the first base and offset address values (see col. 4, lines 65-67, wherein the virtual address does not access the external memory and thus it is not using a memory address to corresponding to the base and offset to access memory).

18. As to Claims 3, 13, Hesson taught detecting a second instruction that stores data into a second memory location that was previously read from without using a memory address corresponding to the second base and offset address values (see store address being compared to all load addresses in col.6, lines 13-15 and 35-41, wherein without using a memory address corresponding to the second base and offset address values is understood to mean without using the base and offset address values to access memory location).

19. As to claims 6, 7, 16, 17, Hesson's virtual addresses were examined to access memory location (see virtual address in col.4, lines 64-67).

20. As to claim 8, 9, 18, 19, examiner holds that virtual same address must have identical base and identical offset.

21. As to claim 10, 11, Hesson also taught a bypass element [violation condition] capable of sending a bypass signal to an instruction execution stage of pipelined microprocessor that indicates that instructions referred to an identical memory location (see store violation condition detected in co1.6, lines 35-42).

22. As to claims 20, Hesson also taught at least
a) detecting a first instruction that stores data to a first memory location, said first instruction comprising syntax (see virtual address comparison) for computing an effective address for the first memory location and the operands needed to compute the effective address in (see the store instruction for the first instruction in store barrier hit detection in col. 5, lines 3-13, see the virtual addresses as the syntax);
b) detecting a second instruction that loads data from a second memory location, the second instruction comprising syntax for computing an effective address for said second memory location (see the snoop of the load instruction as the second instruction in col.6, lines 13-21).

23. Hesson did not explicitly show the determination of syntax relationship between the first memory location and said second memory location, without using the effective address per se as argued by applicant. However, Hesson teaches without using the effective address for the first memory location or the effective address for the second memory (see co1.4, lines 56-67, co1.5, lines 1-13). As explained in the response to

arguments, "*using the effective address for the first memory location*" is interpreted as using the effective address to access memory location.

24. As to the detection of the instructions, examiner holds that for the purpose of detecting the load/store conflicts, Hesson must detect the op code of an instruction to see whether it was a load or store instruction, and virtual addresses by the instructions must comprise a syntax for computing effective address of memory location.

25. As to claim 21, Hesson was also directed to identical memory location (see the address conflicts in col.6, lines 3-29).

Response to Arguments

26. Applicant's arguments filed 12/16/2008 have been fully considered but they are not persuasive.

27. **Appellant's Argument**:

"Independent claims 2, 12 and 20 each recite using base and offset address values, or a syntax, corresponding to an effective address for instructions to determine if the instructions relate to the same memory location, without using the address corresponding to the base and offset address values or syntax. Such a feature is not found in the cited reference. The cited portion *of Hesson* teaches using virtual addresses, not the address tag and offset corresponding to the virtual addresses and without using the virtual addresses."

Examiner's Response:

The examiner respectfully disagrees. The initial limitation "*without requiring computation of the effective address for said memory location"* was more narrower then "*without using the effective address for said first memory location or the effective address for the second memory location"* because the new amended limitation "*without using the effective address for said first memory location...."* is reasonably interpreted as without using the effective address for accessing the memory.

The applicant argues that Hesson fails to teach "*without using the effective address".* However the applicant is reminded that what is claimed is not "*without using effective address*" per se as argued, but "without using the effective address for the first memory location which is interpreted as without using the effective address for accessing the memory location. Therefore, the effective address can be calculated and used for computation but before used to access memory also reads on the claim because the claim limitation is interpreted as using the effective address for accessing the memory location. So, the effective address can be used but not for accessing the memory location reasonably reads on the claim limitation.

Conclusion

28. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Ameson et al. (5,475,823) is cited for the teaching of detection circuit [520] detecting the load instruction accessing a location previously stored (see fig.5, 4, lines 55-67, co1.8, lines 10-24, lines 37-48);

b) Kiyohara et al. (5,694,577) is cited for the teaching of comparison of virtual addresses of preload instructions and store instructions (see co1.2, lines 55-65, co1.5, lines 49-61);

c) Ball (5,615,357) is cited for disclosure of a system including a determination of syntax relationship (see the model of CPU) without itself calculating effective addresses of the first a and second instructions (see the trace file containing the load and store instruction effective addresses in co1.2, lines 39-45, lines 64-67, col.3, lines 1-6, co1.4, lines 1-11, co1.11, lines 59-67, see co1.10, lines 10-52 for the trace driven mode, see co1.12, lines 1-7 for load and store).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDRISS N. ALROBAYE whose telephone number is (571)270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Idriss Alrobaye
AU 2183
(571) 270-1023